40 Gb/s 4:1 Multiplexer and 1:4 Demultiplexer IC Module using SiGe HBTs

Toru Masuda, Ken-ichi Ohhata†, Nobuhiro Shiramizu, Eiji Ohue, Katsuya Oda, Reiko Hayami, Hiromi Shimamoto†, Masao Kondo, Takashi Harada††, and Katsuyoshi Washio

Central Research Laboratory, Hitachi, Ltd., Kokubunji, Tokyo 185-8601, Japan
†Musashino Office, Hitachi Device Engineering, Co. Ltd., Kokubunji, Tokyo 185-8601, Japan
††Device Development Center, Hitachi, Ltd., Ome, Tokyo 198-8512, Japan

***Abstract* — A 4:1 multiplexer and a 1:4 demultiplexer IC module were developed by using 0.2-μm self-aligned selective-epitaxial-growth SiGe HBTs. For the data retiming, the multiplexer and the demultiplexer include a frequency divider that operates at over 40 GHz. 50-Gb/s operation for the multiplexer and 48-Gb/s operation for the demultiplexer were observed by measurements using on-wafer probes. We concluded that these modules, which mounted the IC on a ceramic substrate with a brass block, are applicable to transmitter and receiver functions of a 40-Gb/s optical transmission system.**

I. Introduction

The rapid growth of multimedia communication use demands an expansion of the present transmission capacity. The development of a 40-Gb/s optical transmission system is an effective solution to meet the demand. The ICs used in the systems must be capable of operation at that bit-rate, but must also be sufficiently inexpensive for widespread commercial use. Because of its high speed and high level of integration, the SiGe heterojunction bipolar transistor (SiGe HBT) is an attractive low-cost candidate for such an application. To realize a 40-Gb/s optical transmission system (Fig. 1), we have developed a 0.2-μm self-aligned selective-epitaxial-growth (SEG) SiGe HBT and have reported the development of a 40-Gb/s 1:4 demultiplexer whose performance was measured by using on-wafer probes [1,2]. In broadband optical transmission systems, the high-speed time-division multiplexer (MUX) and demultiplexer (DEMUX) are the key components that strongly need further developing by using SiGe technology. There is a tendency to increase the integration of MUX and DEMUX in a chip. To date, the highest reported performance of a 2:1 MUX was 80 Gb/s on a wafer [3], and 60 Gb/s on a test fixture [5]. And that of a 1:2 DEMUX was 40 Gb/s on a wafer [4] and 60 Gb/s on a test fixture [6]. The highest reported four channel DEMUX achieved was a 40-Gb/s operation on a test fixture [7]. However, none of these MUXs and DEMUXs satisfies both the four channel operation necessary for large-scale SONET/SDH manufacturability and full-clock operation. In this paper, we describe a 4:1 MUX IC module and a 1:4 DEMUX IC module that can be operated at 40 Gb/s with a 40-GHz clock. These four channel IC modules achieved the best performance ever reported.

II. Device Characteristics

We used 0.2-μm self-aligned selective-epitaxial-growth SiGe HBT technology for fabricate the IC [1]. An SEM cross-sectional view of the SiGe HBT is shown in Fig. 2. To provide a good link between the intrinsic and extrinsic base, we used a poly-Si-assisted self-aligned SEG (PASS) structure. The PASS structure enabled both low base resistance and low collector capacitance. Shallow-trench (0.4 μm deep) and dual 0.6-μm-wide deep-trench (3 μm

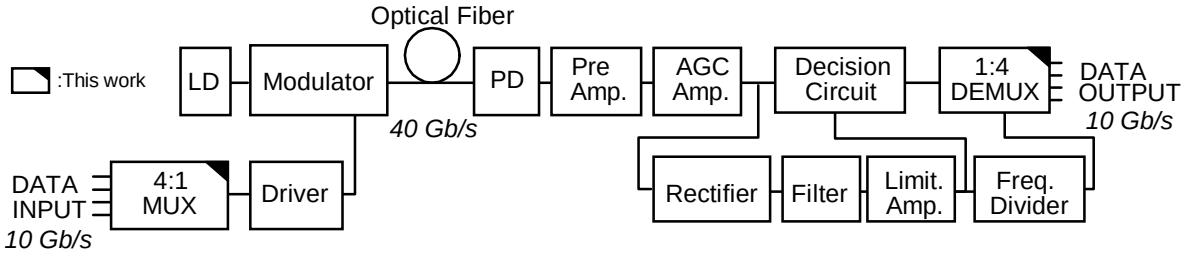

Fig. 1. 40-Gb/s optical transmission system.

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deep) isolations were used to reduce the parasitic capacitance of the collector and substrate. Table I shows the typical transistor parameters. The peak cut-off frequency (f_T) and the peak maximum oscillation frequency (f_{max}), for a SiGe HBT with a 0.2 x 2.0-μm emitter area at a collector-to-emitter bias voltage of 2 V, were 122 and 163 GHz, respectively, at a collector current density of 7.5 mA/μm^2. The minimum differential ECL gate-delay time was 5.5 ps when the internal single-ended voltage swing was set to 250 mVpp.

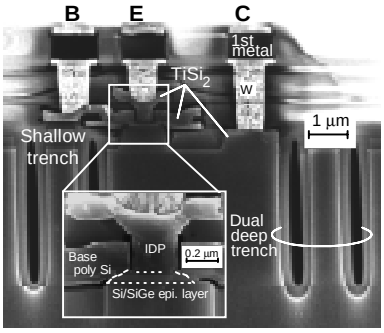

Fig. 2. SEM cross-sectional view of a 0.2-μm SiGe HBT.

Table I. Transistor parameters.

A_E = 0.2 x 2.0 μm		
h_{FE}	1400	
BV_{CER}	3.0	V
R_B	90	Ω
C_{jC}	3.6	fF
C_{SUB}	1.8	fF
f_T	122	GHz
f_{max}	163	GHz

III. Multiplexer

Figure 3 shows the block diagram of the 2:1 multiplexer (2:1 MUX) that is the core circuit of the 4:1 multiplexer. Since both the positive and the negative edges of a clock signal are used for clocking in a selector, the second bit (D2 in selector) is required to be delayed one-half clock period to maximize the phase margin between the input data transitions and the select clock (S in selector). This requirement is fulfilled by using a master-slave D-FF (MS-DFF) for the first bit and a master-slave-slave D-FF (MSS-DFF) for the second bit. Figure 4 shows the block diagram of the 4:1 multiplexer (4:1 MUX). It consists of three 2:1 MUXs connected in a tree structure, an output MS-DFF, an output buffer, and two master-slave T-FFs

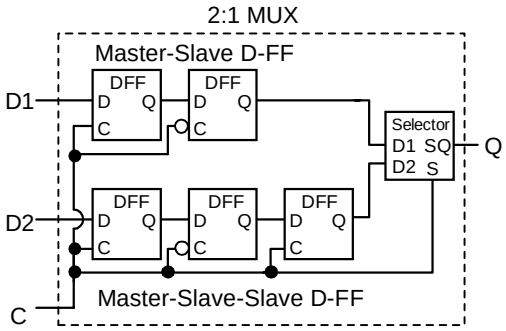

Fig. 3. Block diagram of a 2:1 multiplexer

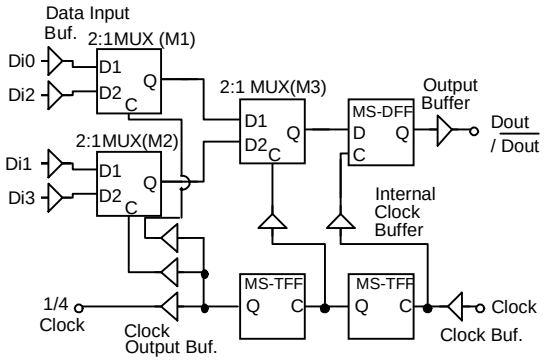

Fig. 4. Block diagram of a 4:1 multiplexer.

(MS-TFFs) in series. If the output MS-DFF is not used, the clock signal for the 2:1 MUX (M3) needs to have a precise 50% duty cycle. However, it is difficult to have a clock whose rising time (tr) and falling time (tf) are equalized. Therefore, to allow for the duty variation of the clock and eliminate any output jitter of the selector in M3, an output MS-DFF was used for retiming using the positive edge. To provide clock signals with proper voltage swing to 2:1 MUX and MS-DFFs, cascoded amplifiers are used in the internal clock buffers.

A photomicrograph of the 4:1 MUX is shown in Fig. 5. The chip was 1.8 x 2.2 mm. The 550- x 950-μm area circuit core was arranged at the center of the chip. A micro-strip transmission line, formed out of the fourth metal as a signal line and the first metal as a ground plane, connects the signal pad and the circuit core. MIM capacitors with a total capacitance of 700 pF around the circuit core eliminate the interference among the power supply patterns.

Figure 6 shows the output eye diagrams of the 4:1 multiplexer IC for a 40-Gb/s and a 50-Gb/s pseudo-random bit sequence (PRBS) measured by on-wafer probes. Well-opened eye diagrams with an output swing of 400 mVpp were obtained. The upper limit for measuring was set to 50 Gb/s because of the 12.5-Gb/s maximum operation speed of the pulse pattern generator.

The total power consumption was 3.2 W at a supply voltage of -5.2 V.

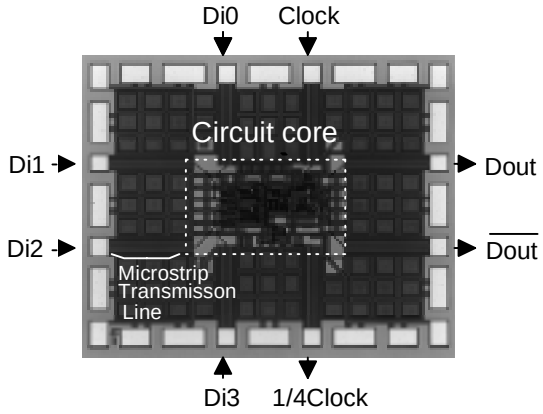

Fig. 5. Photomicrograph of a 4:1 multiplexer.

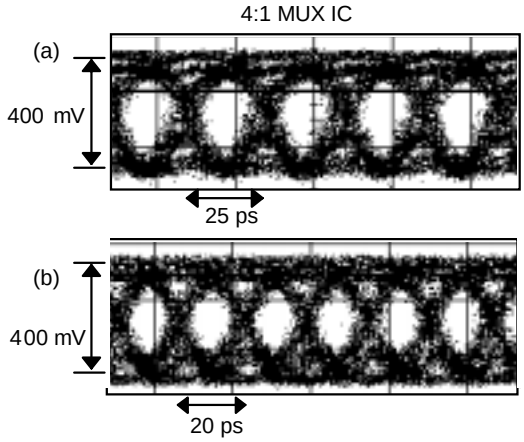

Fig. 6. Output waveform of a 4:1 multiplexer. (a) at 40 Gb/s, and (b) at 50 Gb/s.

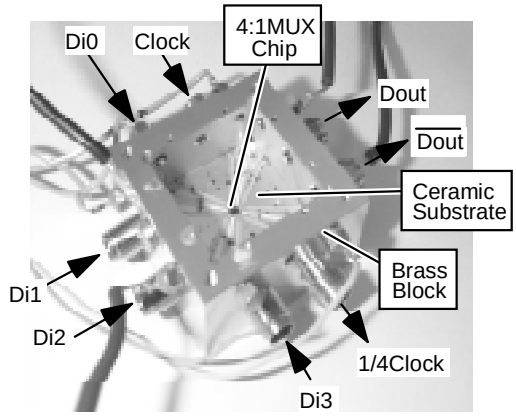

Fig. 7. Photograph of a 4:1 multiplexr IC module.

A photograph of the 4:1 MUX IC module is shown in Fig. 7. The IC module consisted of a ceramic substrate soldered on a CuW spacer and a brass block with co-axial connectors. The IC chip was glued onto the spacer and ultrasonically bonded to the co-planer line on the ceramic substrate at the same level. Figure 8 shows the output waveforms for a 48-Gb/s PRBS and a known data pattern input of the 4:1 multiplexer IC module. The waveforms were measured via a 1-m co-axial cable. The voltage swing was 300 mVpp, the rise and fall times (20-80%) were 15 and 17 ps, respectively.

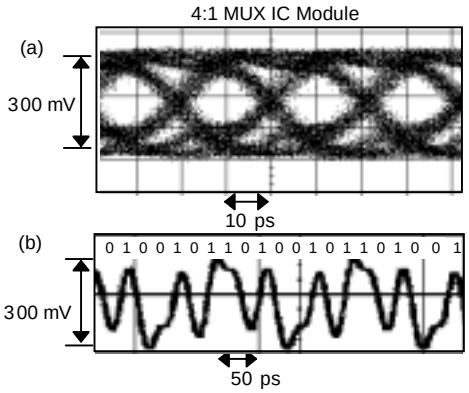

Fig. 8. Output waveform at 48 Gb/s of a 4:1 multiplexer module. (a) a PRBS data pattern, and (b) a known data pattern.

IV. Demultiplexer

We already presented a 40Gb/s 1:4 DEMUX with a decision circuit [2]. In this work, the current of clock input buffer was optimized in order to increase maximum operation speed of the 1:4 DEMUX. Furthermore, as same as the 4:1 MUX, the evaluation as an IC module was carried out. Figure 9 shows the block diagram of the 1:4 DEMUX. The 1:4 DEMUX consists of a MS-DFF, three 1:2 DEMUXs, and a clock-distribution circuit (CDC). A MS-DFF for data retiming is used in front of the first 1:2 DEMUX. A 1:2 DEMUX is composed of a MS-DFF and a MSS-DFF. In the CDC, byte-synchronization is enabled by bit-rotation. The CDC controls the phase relationship between 1/2 clock (CKA) and 1/4 clock (CKB) by the four states of the two EX-OR's output, which are determined from the bit-rotation signal via two 2-bit counters in series. Therefore, only one bit-rotation signal is needed to change the data until the output-bit pattern of the 1:4 DEMUX becomes properly aligned. Figure 10 shows the output waveforms at 48 Gb/s measured by on-wafer RF probes. Clear demultiplexed output data patterns (Do1-Do3) of 400 mVpp at 12 Gb/s were obtained. The power supply

voltage was -5.2 V, and the power consumption was 3.2 W for a 1.8 x 2.2-mm chip.

We observed error-free operation of the 1:4 DEMUX module at 40 Gb/s. The measured input phase margin was 202 ° and input sensitivity was 115 mVpp. Furthermore, we evaluated the optical transmission system with the 4:1 MUX IC module and the 1:4 DEMUX IC module at 40 Gb/s (back to back measurement). A receiver sensitivity of -22 dBm was obtained at 10^{-9} BER [8]. These results show that the performance of both the MUX and the DEMUX IC modules were sufficient for use in practical 40-Gb/s optical transmission systems.

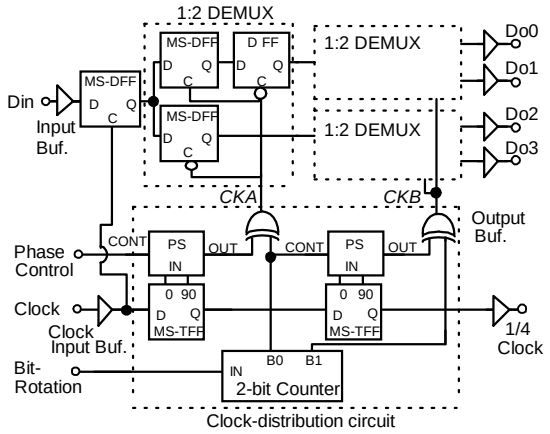

Fig. 9. Block diagram of a 1:4 demultiplexer.

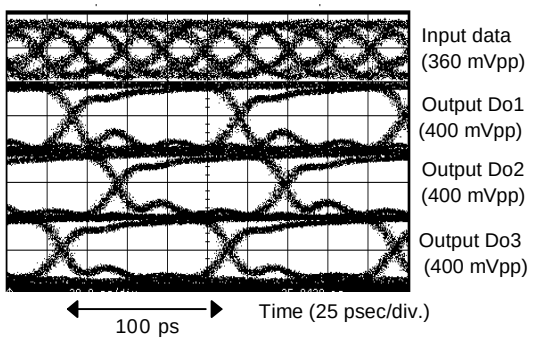

Fig. 10. Output waveform of a 1:4 demultiplexer at 48 Gb/s.

V. Conclusion

A 4:1 MUX IC module and a 1:4 DEMUX IC module were developed by using 0.2-μm self-aligned selective-epitaxial-growth SiGe HBTs. A SiGe HBT with a cut-off frequency of 122 GHz is attributed to the minimum ECL gate-delay time of 5.5 ps we obtained. Thus, the MUX and the DEMUX can include a frequency divider that operates at over 40 GHz and allows full-clock operation. We observed 50-Gb/s operation for the MUX and 48-Gb/s operation for the DEMUX by using RF wafer probes. As a result of the evaluation of optical transmission system with the MUX/DEMUX IC module, it was shown that these IC modules are applicable to transmitter and receiver functions for a 40-Gb/s optical transmission system. These results of the 4:1 MUX IC and IC module are the best performance ever reported for four channel MUX. The 1:4 DEMUX IC module also achieved the fastest reported operation. In the future, we will be able to provide a 50-Gb/s MUX/DEMUX module for measurement equipment and all the ICs needed for a 40-Gb/s optical transmission system [9].

Acknowledgement

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